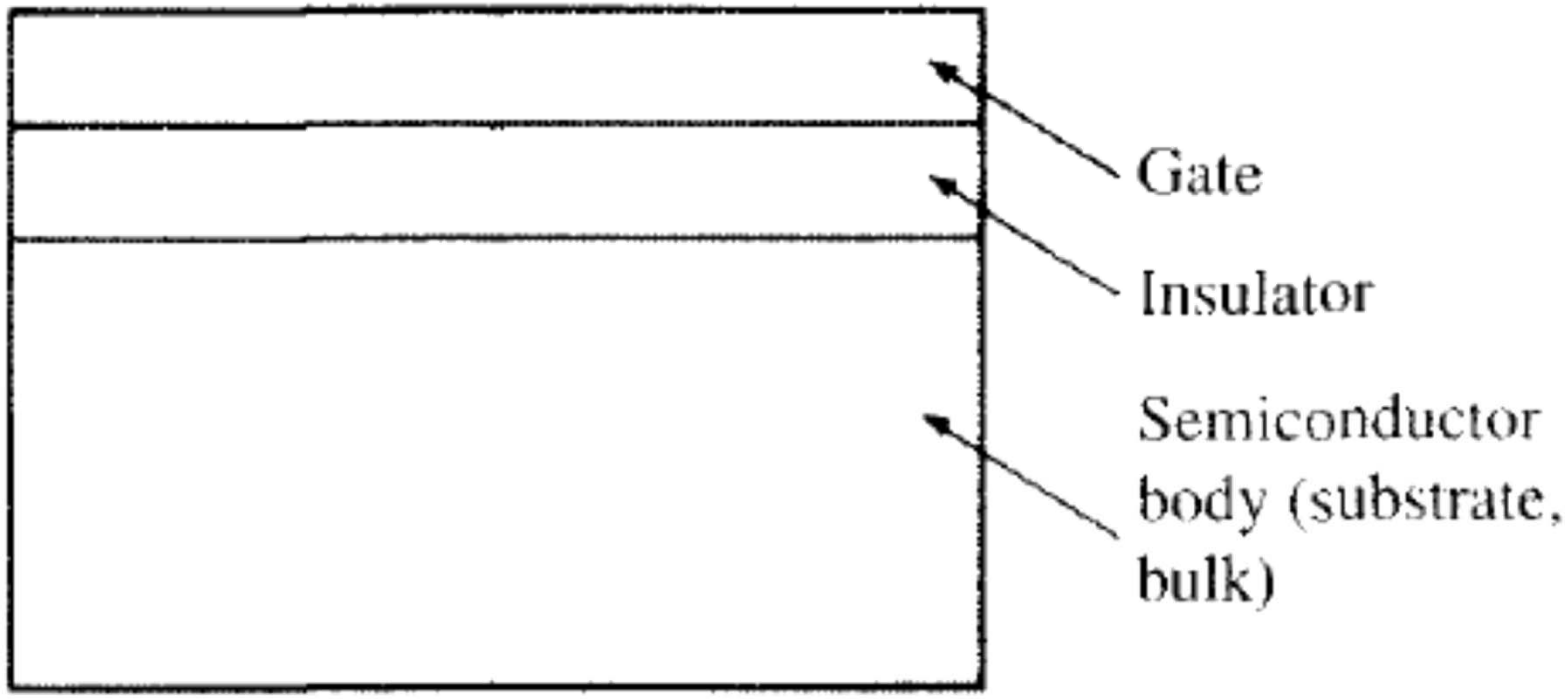
The two terminal MOS structure

Introduction

- The two terminal MOS – MOS capacitor
- Historical background – studied for many years

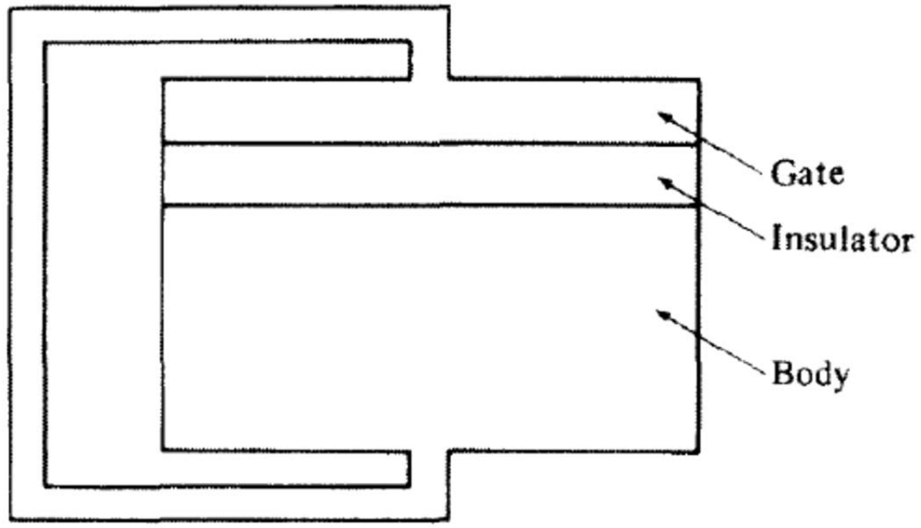


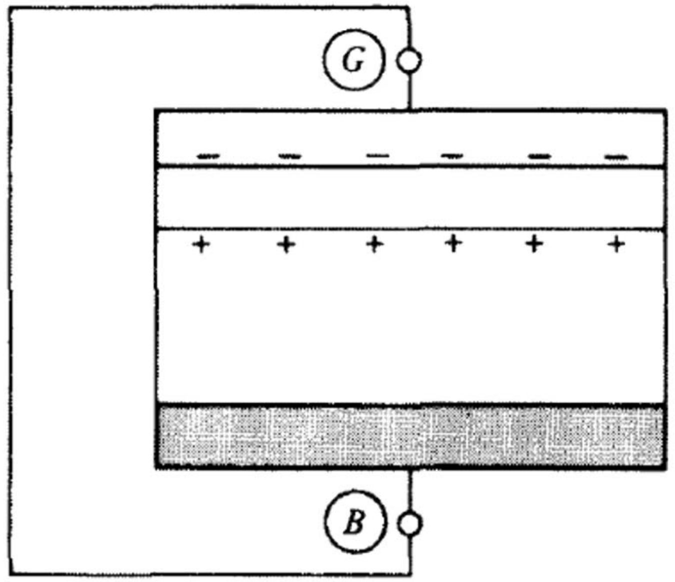
The flatband voltage

The flatband voltage

- Case 1: both gate and body material is same (p-type with same doping concentration)
  - What happen?
    - As the wire is also the same martial as body and gate martial there is no charge pile up anywhere! – martial in neutral everywhere.
    - There will be no electrical field
- Case 2 (more realistic): Gate material is not the same with body material
  - Gate and body have metal contact material and connected to each other with a metallic wire (short circuit)
  - Although there are several contact potential between gate and body but we have:

$$Contact\ potential\ from\ gate\ to\ bulk = \phi_S - \phi_M = \phi_{SM}$$



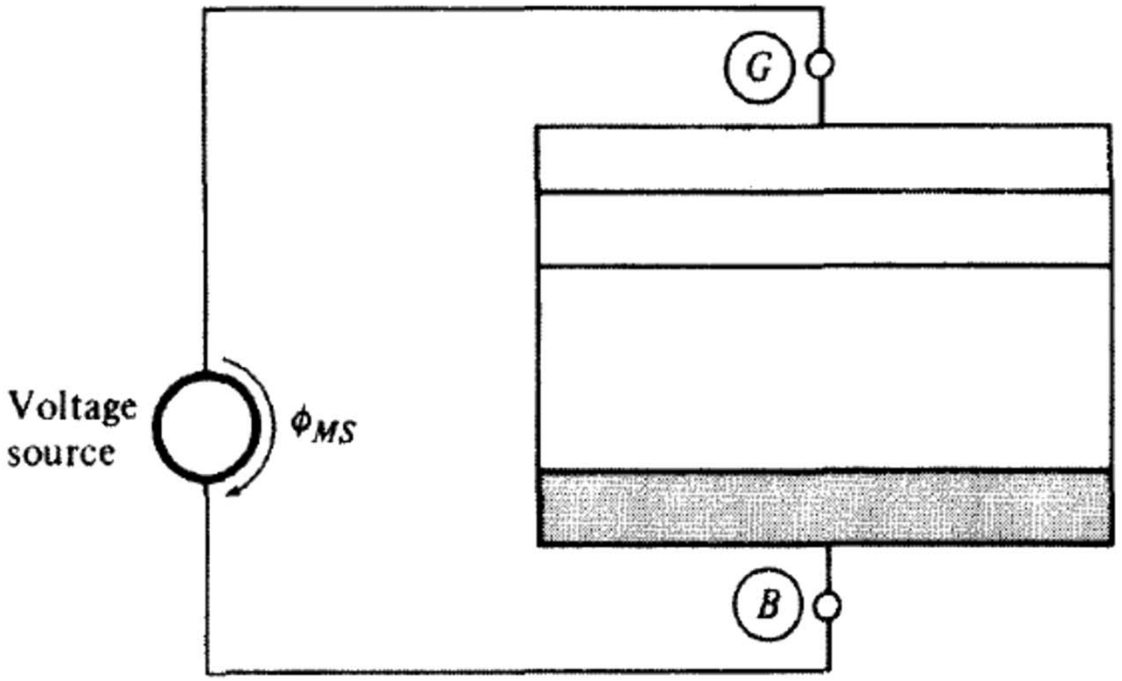


The flatband voltage…

- One can cancel the contact potential by applying the same negative voltage as Φ_{SM}.:

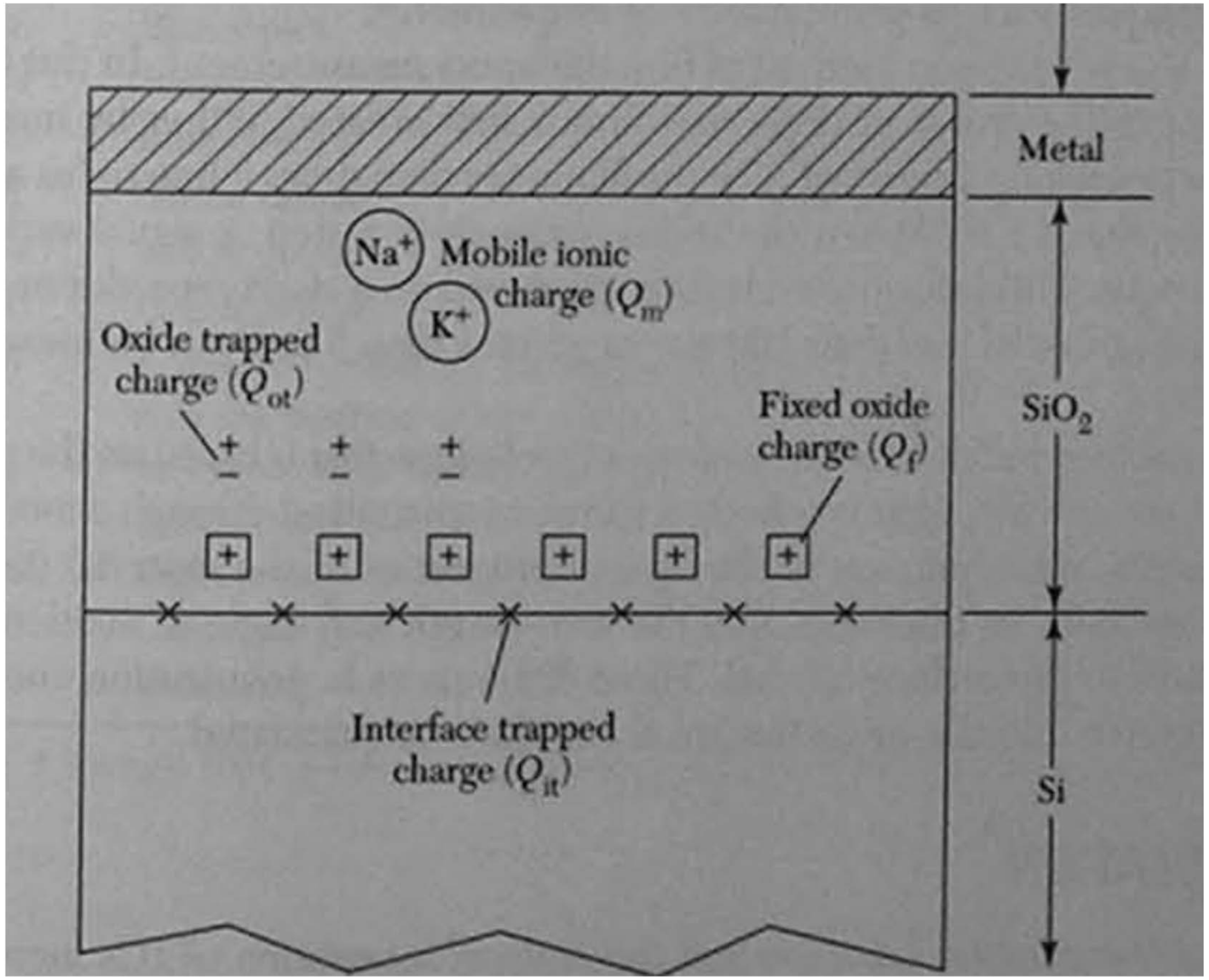
$$\phi_{MS} = \phi_M - \phi_S$$

  - In this condition net flow cancelled and device become neutral.
  - Ex: For different gate materials such as Aluminum, n-type polysilicon and p-type polysilicon calculate the Φ_{MS} If the body material is a given p-type material
    - Aluminum gate: $\phi_{MS} = 4.1 - (4.05 + 0.56 + \phi_F) = -0.51 - \phi_F$
    - n-type polysilicon: $\phi_{MS} = 4.05 - (4.05 + 0.56 + \phi_F) = -0.56 - \phi_F$
    - p-type polysilicon: $\phi_{MS} = (4.05 + 1.12) - (4.05 + 0.56 + \phi_F) = 0.56 - \phi_F$



The flatband voltage…

- Parasitic charge in oxide
  - Fixed oxide charge
    - Independent of oxide thickness and body doping concentration
    - Due to uncompleted bound between Si-Si and Si-O
    - 1-3nm above the surface
    - Dependent to crystal orientation
  - Oxide trapped charge
    - Made by irradiation, photoluminescence or high voltage
  - Mobile ionic charge
    - Due to environmental contamination– fabricating through the hand
    - These charges can move in oxide due to electric field
  - Interface trapped charge
    - Defects at surface – SiO2/Si
    - Act like donor or acceptor
    - Crystal orientation dependent
- It is too hard to control them – undesirable effects



The flatband voltage…

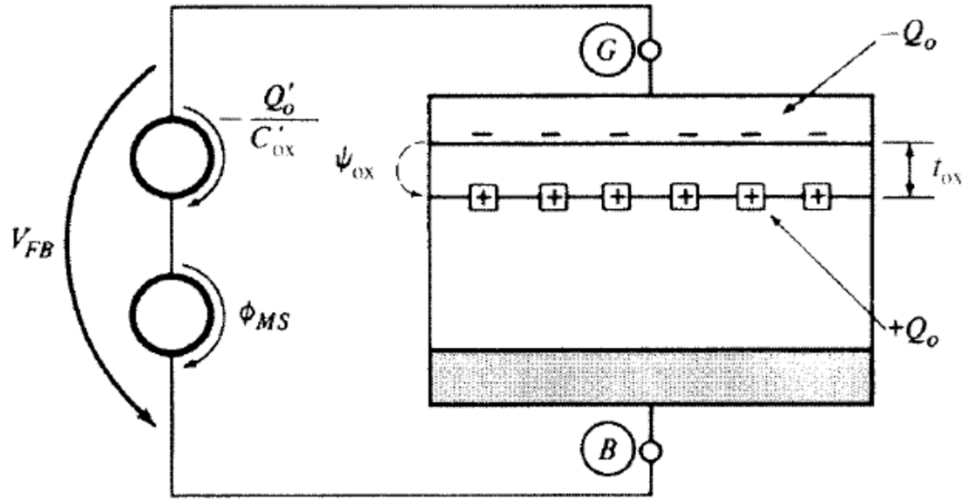
- Effective interface charge : Q_0
  - In todays devices Q_0 is almost always positive
  - It is between 1.6×10^{-9} to 1.6×10^{-8} C/cm² which is corresponds to 10^{10} to 10^{11} ions/cm² effective interface ion density
  - Potential drop across the oxide : ψ_{ox}

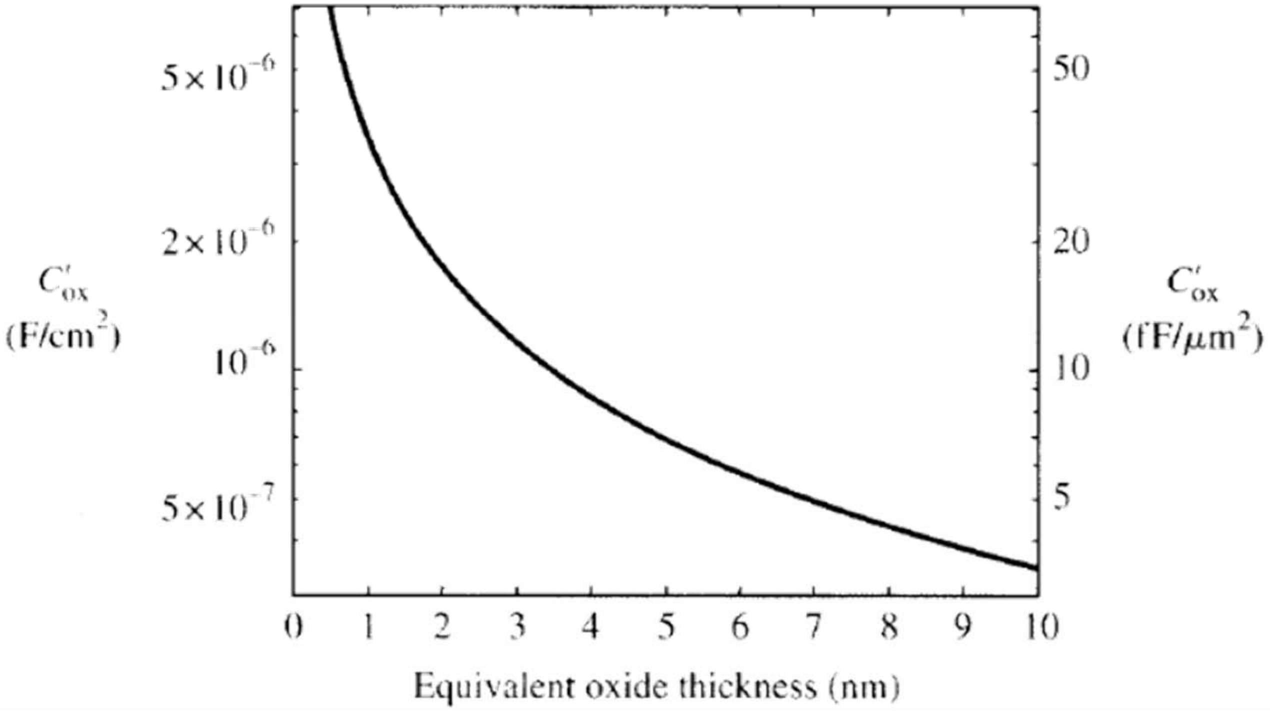
$$\psi_{ox} = -\frac{Q_0}{C_{ox}} = -\frac{Q_0'}{C_{ox}'}$$

$$C_{ox}' = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$\varepsilon_{ox} = k_{ox}\varepsilon_0 \,, k_{ox} = 3.9 \; for \; SiO_2$$

  - In new modern devices other oxide can be used





The flatband voltage…

- Flat band voltage: V_{FB} – Flat energy band between gate and body

$$V_{FB} = \phi_{MS} - \frac{Q_0'}{C_{ox}'}$$

- In modern devices second term can be negligible!
- Ex: Calculate the flatband voltage for a p-type body semiconductor with $N_A=10^{18}/cm^3$, n-type polysilicon with $N_D=10^{18}/cm^3$ and a Sio2 insulator with 2nm thickness and $Q_0'=10^{-8} C/cm^2$

$$\phi_F \approx KTln\left(\frac{N_A}{n_i}\right) = 0.476\,V$$

$$\phi_{MS} = -0.56 - 0.476 = -1.036\,V$$

$$C_{ox}' = \frac{\varepsilon_{ox}}{t_{ox}} = 1.73 \times 10^{-7}\,F/cm^2 \Rightarrow \frac{Q_0'}{C_{ox}'} = 0.006\,V$$

$$V_{FB} = \phi_{MS} - \frac{Q_0'}{C_{ox}'} = -1.036 - .006 = 1.0412\,V$$

The flatband voltage…

- Illustration
- $\phi_M > \phi_S$
- Fermi level in metal and semiconductor should line up in equilibrium state – potential drop across the device! Led to carrier movement.
- To prevent from this movement external voltage source should apply to cancel out built in potential

$$V_{GB} = V_{FB} = \phi_{MS} - \frac{Q'_0}{C'_{ox}}$$