The Four-Terminal MOS Transistor

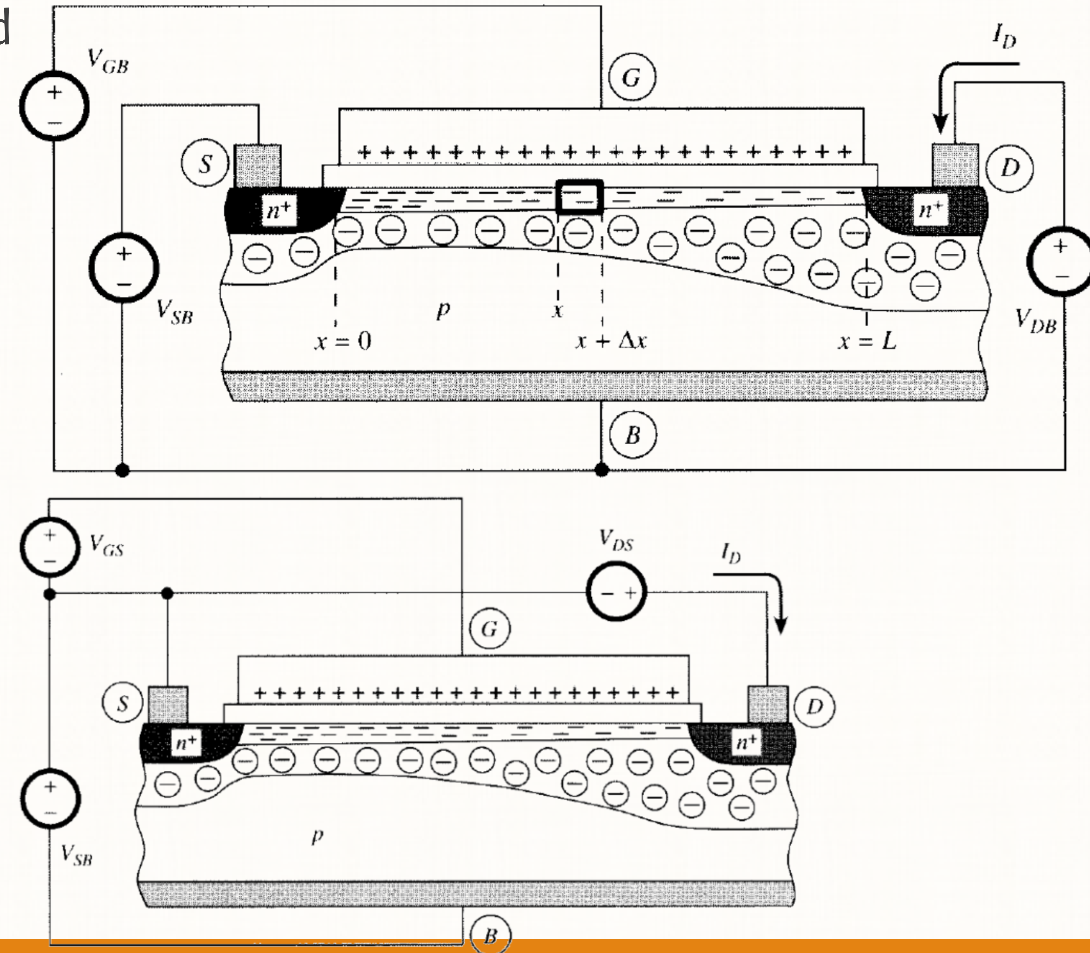
Introduction

- The MOS transistor is obtained by adding one more terminal to the structure of 3 terminal MOS, so that the inversion layer is contacted at two opposite ends.
- By applying a **voltage between these ends**, a ***current*** can be caused to flow in the inversion layer.
- Since the **density of carriers** available for conduction depends on the ***gate potential***, the latter can be used to either create or eliminate the inversion layer (i.e., turn the device "on" or "off") for digital applications or to modulate its conduction in a continuous manner for analog applications.
- The basic theory of MOS transistor operation was developed in the early 1960s.
- Our goal will be to determine the drain current for any combination of DC terminal voltages.
- Some assumptions:
  - channel is sufficiently *long* and *wide* → *No edge effect*
  - substrate is *uniformly* doped (p type)
  - *Steady state condition*

Introduction…

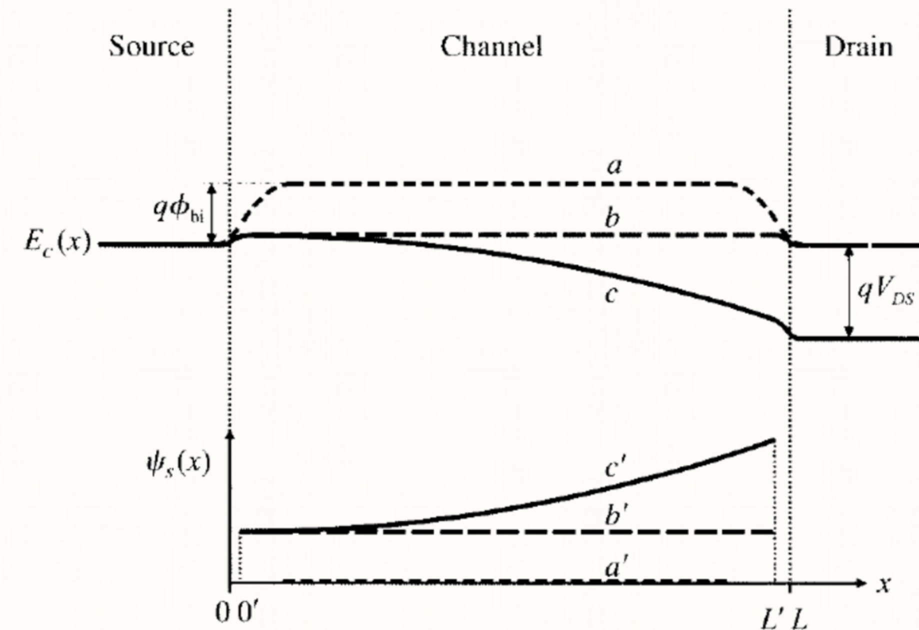
- An nMOS transistor with external de voltages applied is shown in Fig.
- Common body connection preview (up)
- Common source connection (down)
- Three terminal MOS can be used here
  - Source end channel if $V_{CB} = V_{SB}$
  - Drain end channel result if $V_{CB} = V_{DB}$
- It should be emphasized that *normal operation of a MOS transistor requires that* ***both pn junctions he reverse-biased****. So that:*

$$V_{SB} \geq 0$$
$$V_{DB} \geq 0$$



Introduction…

- A simple energy band diagram at the surface, as shown in Fig. First assume $V_{SB} = 0$ and $V_{DB} = V_{SB}$.
- First case (a) $V_{SB} = 0$, $V_{DB} = V_{SB}$ and $V_{GB} = V_{FB}$ → no inversion layer
  - The total variation of E_C is equal to $q\phi_{bi}$ where ϕ_{bi} is the junction built-in potential. It can be seen that the electrons in the n⁺ regions face an energy barrier of this height, which makes it difficult for them to enter the channel → $\psi_s = 0$.
- Second case (b) $V_{SB} = 0$, $V_{DB} = V_{SB}$ and $V_{GB} \gg V_{FB}$ → Strong inversion regime
  - Surface potential to become positive → Corresponding electron potential energy at the surface of the body will be reduced.
  - The electrons in the n⁺ regions to enter the channel and form an inversion layer.
  - the energy barrier has not been eliminated completely; this is because the surface potential.



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- Third case (c) $V_{DB} > V_{SB}$ and $V_{GB} \gg V_{FB}$
  - $V_{GB} \gg V_{FB}$ →The surface potential is enough to cause strong inversion.
  - $V_{DB} > V_{SB}$ →This raises the surface potential near the drain.
  - Increasing the potential at the drain corresponds to lowering the electron energy there.
  - The direction of the electric field now is such that it causes electrons to move toward the right; a ***channel current results***.
  - Channel length: As shown in previous figure we have transition region based on applied voltages:

$$0 \rightarrow 0'$$

$$L \rightarrow L'$$

  - This change have considerable effect on short channel MOS. But here we ignore it as the device length in long.

- Some assumptions:
  - The oxide and the depletion region under the channel as perfectly insulating layers → $I_G = 0$, $I_B = 0$
  - No drain body leakage current → $I_{DS} = I_D$
    - These assumptions are not correct for small dimension devices

- Charge density uniformity is no longer take place in channel. (Fig. & Fig.) for small ΔA→ $Q_{I,B,G} = \frac{\Delta Q_{I,B,G}}{\Delta A}$