Theory and Technology of Semiconductor Fabrication

By Mohammad Razaghi

Course description

- Instructor:

Dr. Mohammad Razaghi
Assistant Professor
Electrical Engineering Department
Faculty of Engineering
University of Kurdistan
Email: m.razaghi@uok.ac.ir
Homepage: http://eng.uok.ac.ir/razaghi/

Course description (Cont.)

- Textbooks
  - ***Fundamentals of Semiconductor Fabrications***, Gray S. May and Simon M. Sze, John Wiley and Sons,2004
  - ***Modular series on Solid State Devices, Volume V, Introduction to Microelectronic Fabrication***, Richard C. Jager, Addison-Wesley Publication
  - ***Semiconductor Devices, Physics and Technology, Second Edition***, Simon M. Sze, John Wiley and Sons ,2002

Course description (Cont.)

- Syllabus
  - Introduction
  - Crystal Growth
  - Silicon Oxidation
  - Photolithography
  - Etching
  - Diffusion
  - Ion Implantation
  - Film deposition
  - Process Integration

Course description (Cont.)

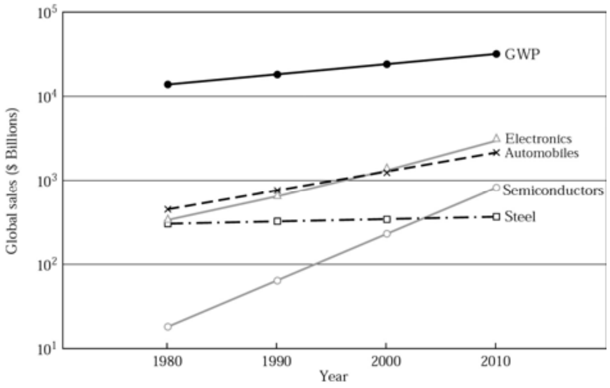
- Grading
  - 20% Project
  - 20% Seminar
  - 60% Final Examination

Introduction

Introduction

- Semiconductor devices are the foundation of electronic industry, which is the *largest industry* in the world.
- The multitrillion dollar electronic industry is fundamentally dependent on the manufacture of semiconductor integrated circuits (ICs).
- *Telecommunications*, *aerospace*, *automotive* and *consumer electronic industries* all rely on semiconductor devices.
- Therefore basic knowledge of semiconductor *materials, devices and processes* is essential to understanding of modern electronic.

Introduction (Cont.)



Gross world product (GWP) and sales volume of the electronics, automobile, semiconductor, and steel industries from 1980 to 2000 and projected to 2010

Semiconductor Materials

- *Germanium* (Ge) → First transistor (1947)
- Ge was rapidly replaced by *Silicon* (Si) in 1960 because:
  - It is the *primary constituent* of ordinary sand → make it very inexpensive
  - It can be easily oxidized to form a high quality s*ilicon dioxide* (SiO2) insulator → Excellent barrier layer for selective diffusion steps needed in IC fabrication.
  - It has a *wider bandgap* than Ge → It can operate at higher temperature

Semiconductor Materials (Cont.)

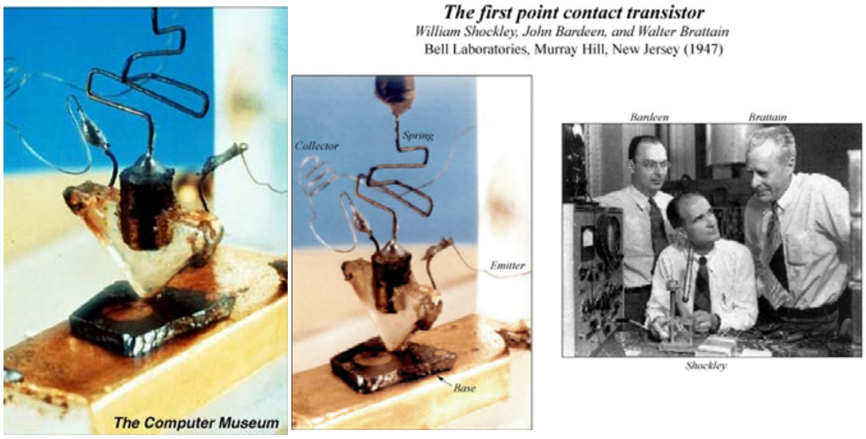
- GaAs → It has *higher electron mobility* than Si → high speed devices
- *Direct bandgap material* → Laser & LED
- Major drawbacks:
  - Less stability during thermal processing
  - Poor native oxide
  - Higher cost
  - Much higher defect density

Semiconductor devices

Semiconductor devices

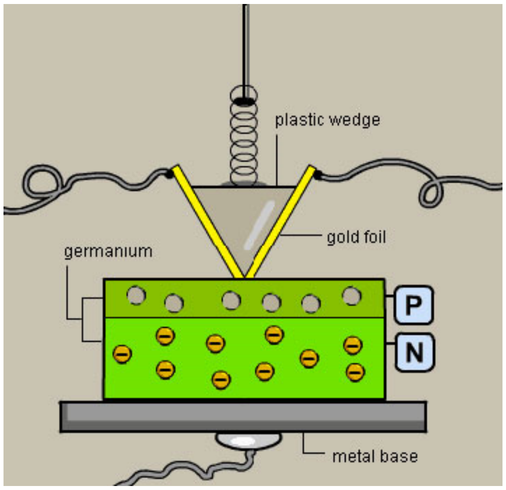
- Semiconductor devices has been studied for more than 130 year.
- *Metal-semiconductor contact* → Braun (1874). Resistance between metal and metal sulfide depended on magnitude and polarity of the applied voltage.
- *Light emitting diode (LED)* → Round (1907) → Yellowish light from Silicon Carbide (SiC) crystal by applying 10 V potential voltage.
- *Bipolar transistor* → Bardeen, Brattain & Shockley (1947).
- …

Bipolar transistor



The first transistor. (Photograph courtesy of Bell Laboratories)

Bipolar transistor (Cont.)



MOSFET

- The *most important* device for advanced integrated circuits is the MOSFET (Metal Oxide-Semiconductor Field-Effect Transistor) which was first reported by Kahng and Atalla in 1960.
- Although present day MOSFET have been scaled down to the deep submicron regime. the choice of *silicon* and *thermally grown silicon dioxide* used in the first MOSFET remains the most important combination of materials.
- The MOSFET and related integrated circuits now constitute about 90% of the semiconductor device market. An ultra small MOSFET with n channel length of 15 nm has been demonstrated recently. This device can serve as the basis for the most advanced integrated circuit chips containing over *one trillion* devices.

MOSFET (Cont.)

The first MOSFET. (Photograph courtesy of Bell Laboratories) 20 um gate length and 100 nm oxide thickness

Major Semiconductor devices

Year	Semiconductor device	Inventor(s)
1874	Metal semiconductor contact*	Braun
1907	Light emitting diode (LED)*	Round
1947	Bipolar transistor (Nobel)	Bardeen, Brattain & Shockley
1949	p-n junction*	Shockley
1952	Thyristor	Ebers
1954	Solar cell*	Chapin, Fuller & Pearson
1957	Heterojunction bipolar transistor	Kroemer
1958	Tunnel diode*	Esaki
1960	MOSFET	Kahng & Atalla

Major Semiconductor devices

Year	Semiconductor device	Inventor(s)
1962	Laser*	Hall et al.
1963	Heterostructure laser*	Kroemer
1966	MESFET	Mead
1967	Semiconductor memory	Kahng & Sze
1970	Charge coupled-device (Nobel)	Boyle & Smith
1980	MODFET	Mimura
1994	Room temp. memory cell	Yano
2001	15 nm MOSFET	Yu

SEMICONOUCTOR PROCESS TECHNOLOGY

SEMICONOUCTOR PROCESS TECHNOLOGY

- The growth of metallic crystals in a furnace was pioneered by Africans living on the western shores of Lake Victoria more than 2000 years ago.
- Milestone of technology →*Lithography* → Invented in 1798. In this process the pattern or image was transferred from a stone plate (*litho*).

SEMICONOUCTOR PROCESS TECHNOLOGY (Cont.)

- *Czochralski* technique → liquid-solid mono-component growth technique → developed for making *silicon crystal* (1918).
- *Bridgeman* technique → developed for making *GaAs crystal* (1925).
- *Diffusion* technique → developed for *altering* the Si *conductivity* characteristics (1952).
- *Lithography* technique → for the first time used for *semiconductor device fabrication* (1957). It is a *key* technology for semiconductor industry. It is currently representing over *35%* of IC manufacturing cost.

SEMICONOUCTOR PROCESS TECHNOLOGY (Cont.)

- The *oxide masking* method was developed in 1957. They found that an oxide layer can prevent most impurity atoms from diffusing through it.
- In the same year, the *epitaxial growth process* based 0n the chemical vapor deposition technique was developed.
- Epitaxy, derived from the Greek words *epi*, meaning "*on*," and *taxis*, meaning "*arrangement*," describes a technique of crystal growth to form a thin layer of semiconductor materials on the surface of a crystal that has a lattice structure identical to that of the crystal. This method is important for the improvement of device performance and the creation of novel device structures.

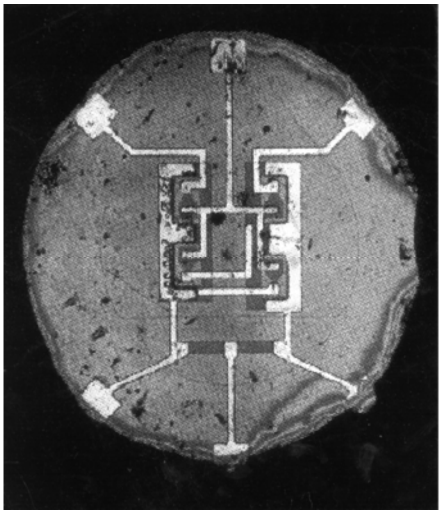
SEMICONOUCTOR PROCESS TECHNOLOGY (Cont.)

- In 1959 a rudimentary *integrated circuit* was made by Kilby. It contained one bipolar transistor, three resistors, and one capacitor, all made in germanium and connected by wire bonding.

- Also in 1959, Noyce proposed the *monolithic IC by fabricating* all devices in a single semiconductor substrate *(monolith means "single stone")* and connecting the devices by aluminum metallization.

SEMICONOUCTOR PROCESS TECHNOLOGY (Cont.)

The first monolithic integrated circuit



SEMICONOUCTOR PROCESS TECHNOLOGY (Cont.)

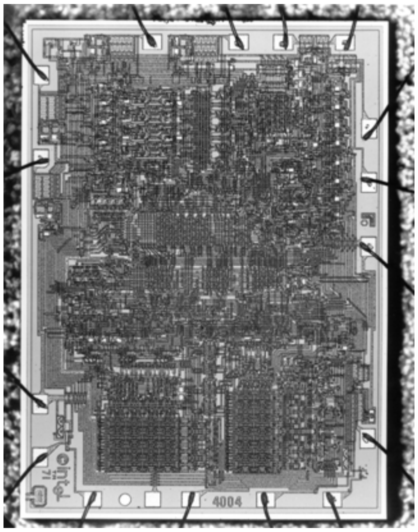
- *CMOS* (Complementary MOSFET) technology (1963) → NMOS and PMOS transistor together → *Logic gate* , minimizing power consumption.
- *DRAM* (Dynamic Random Access Memory) technology – two element circuit (1967) → One transistor and one charge store capacitor → Consume high power.
- *Polysilicon self-aligned gate process* (1969) → improve device *reliability* and reduce *parasitic capacitor*.
- *MOCVD* (Metalorganic chemical vapor deposition) technology (1969) → important *epitaxial growth* technique for compound semiconductors such as *GaAs*.
- *MBE* (Molecular beam epitaxy) technology (1971) → Near perfect vertical *control of composition and doping* down to atomic dimensions. It is responsible for the creation of numerous photonic devices and quantum-effect devices.

SEMICONOUCTOR PROCESS TECHNOLOGY (Cont.)

- In 1971 the first microprocessor was made by Hoff et al. He put the entire *central processing unit* (CPU) of a simple computer on one chip. It was a four bit microprocessor (Intel-4004). It contained 2300 MOSFET .
- It was fabricated by p-channel polysilicon gate process using 8 um design rule*. This was a major breakthrough for the semiconductor industry*. Currently microprocessors constitute the largest segment of the industry.
- Since the early 198Os many new technologies have been developed to meet the requirements of over shrinking minimum feature lengths. Three key technologies are *trench isolation, chemical mechanical polishing and copper interconnect*.
- Although aluminum has been used since the early 1960s as interconnect material. it suffers from electromigration at high electrical current. *Copper interconnect* was introduced in 1993

SEMICONOUCTOR PROCESS TECHNOLOGY (Cont.)

The first microprocessor. 3mm*4mm (Photograph courtesy of Intel Corp.)



Technology Trends

Technology Trends

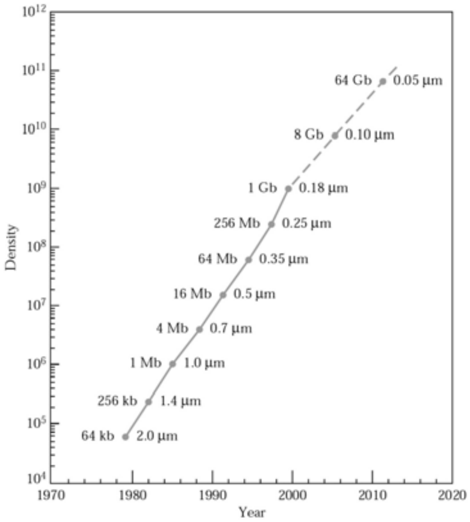
- From the beginning of the microelectronics era the smallest linewidth (or the minimum feature length) of an integrated circuit has been reduced at a rate of about 13% per year.
- At that rate the minimum feature length will shrink to about 50 nm in the year 2010. Device miniaturization results in reduced unit cost per Circuit function. For example the cost per bit of memory chips has halved every 2 years for successive generations of DRAM circuits.
- As device dimensions decrease, the intrinsic Switching time decreases. Device speed has improved by four orders of magnitude since 1959.

Technology Trends (Cont.)

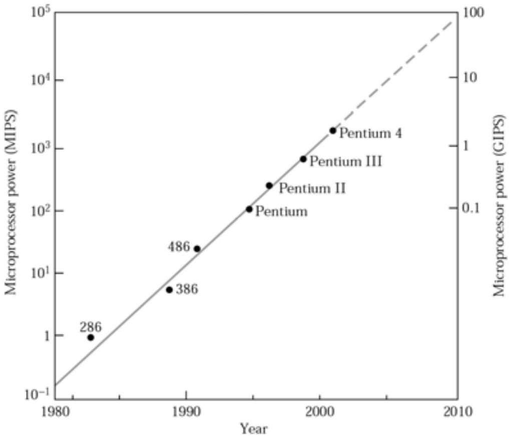
- Higher speeds lead to expanded IC functional throughput rates.
- In the future digital ICs will be able t0 perform data processing and numerical *computation at terabit-per-second rates*.
- As devices becomes smaller, they *consume less power*. Therefore device miniaturization also reduces the energy used for each switching operation.
- *The energy dissipated per logic gate has decreased by over one million times since 1959*.

Technology Trends (Cont.)

Exponential increase of dynamic random access memory density versus year based on the Semiconductor Industry Association roadmap.



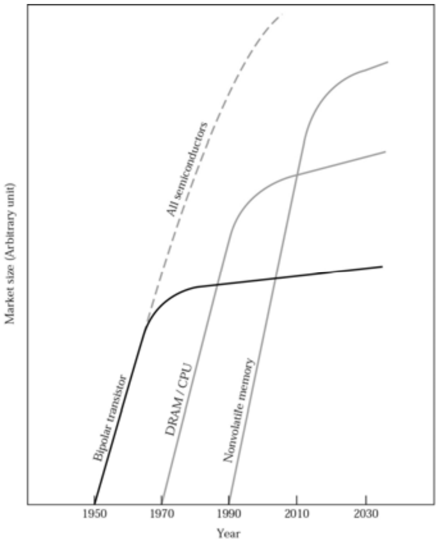
Technology Trends (Cont.)



Exponential increase of microprocessor computational power versus year.

Technology Trends (Cont.)

Growth curves for different technology drivers.



BASIC FABRICATION STEPS

BASIC FABRICATION STEPS

- Today, planar technology is used extensively for fabrication.
- the *major steps* of a planar process steps
  1. *Oxidation*
  2. *Photolithography*
  3. *Etching*
  4. *Ion implantation*
  5. *Metallization*

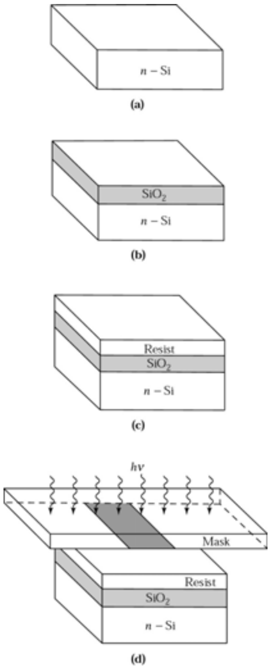
---

a) A bare *n*-type Si wafer.

b) An oxidized Si wafer by oxidation.

c) Application of resist.

d) Resist exposure through the mask.



a) The wafer after the development.

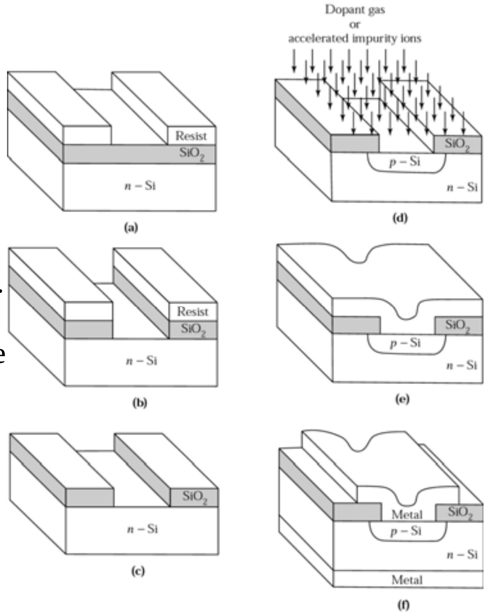
b) The wafer after SiO_2 removal.

c) The final result after a complete lithographic process.

d) A *p*-*n* junction is formed in the diffusion or implantation process.

e) The wafer after metallization.

f) A *p*-*n* junction after the complete processes.



Oxidation

- The development of a high-quality silicon dioxide (SiO2) has helped to establish the dominance of Si in the production of *commercial ICs* (Fig).

- Oxidation *advantages*:
  - Insulator in some devices
  - Barrier to diffusion and ion implantation during device fabrication.

- Oxidation *methods*:
  - *Dry → dry oxygen*
  - *Wet → Wet vapor*

Oxidation

- *Dry oxidation* is usually used to form thin oxides in a device structure because of its good Si-SiO2 interface characteristics.
- *Wet oxidation* is used for thicker layer because of its higher growth rate.

Photolithography

- *Photolithography* is used to define the geometry of the p-n junction.
- After the formation of SiO2. the wafer is *coated* with an ultraviolet (UV) light-sensitive material called a *photoresist* which is spun on the wafer surface by high-speed spinner (Fig).
- Afterward the wafer is *backed* about 80˚C to 100 ˚C to *harden the resist for improved adhesion*.

Photolithography (Cont.)

- Next step → *expose* the wafer through the *patterned mask* using a UV-light source. The exposed region of the photoresist-coated wafer under-goes chemical reaction depending on the type of the resist.
- The area exposed to light becomes *polymerized and difficult to remove* in an etchant process. The polymerized region remains when the wafer is placed In a developer. Whereas the *unexposed region* (under the opaque area) *dissolves and washes away* (Fig).

Etching

- *First* step→ The wafer is again *baked* to 120˚C to 180 ˚C for 20 minutes to enhance the adhesion and improve the resistance to subsequent etching process.
- *Second* step→ An etch using hydro-fluoric acid (HF) remove the unprotected SiO2 surface (Fig).
- *Third* step → The resist is stripped away by a chemical solution or an oxygen plasma system.
- After the lithography and etching process the wafer is ready for forming the p-n junction by a diffusion or ion implantation process.

Diffusion and Ion Implantation

- Doping technologies:
  - *Diffusion*
  - *Ion implantation*
- *Diffusion* method → The semiconductor surface not protected by the oxide is exposed to a source with a high concentration of opposite-type impurity. The impurity moves into the semiconductor crystal by solid-state diffusion.
- *Ion implantation* method → the intended impurity is Introduced into the semiconductor by accelerating the impurity ions to a high energy level and then implanting the ions in the semiconductor. The SiO2 layer serves as a barrier to impurity diffusion or ion implantation.
- After the diffusion or implantation process the p-n junction is formed (Fig).

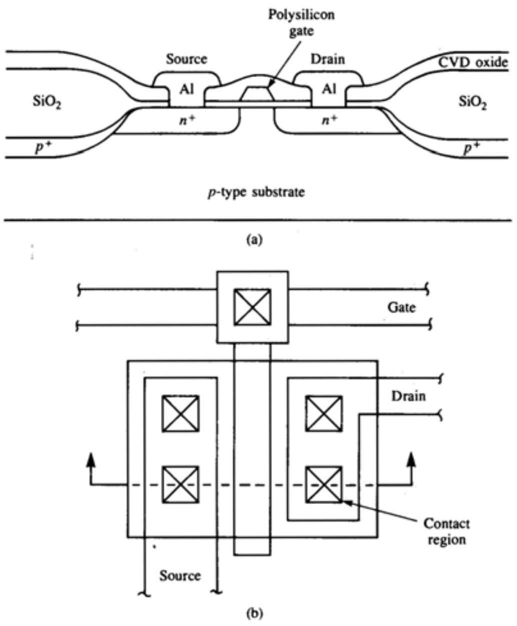
Metallization

- *Metallization* → used to form *ohmic contact* and *interconnections* (Fig).
- Metal films can be formed by physical vapor deposition or chemical vapor deposition.
- The *photolithography* process is again used to define the front contact. A similar metallization step is performed on the back contact without using a lithography process.
- Normally, a low-temperature (< 500 C) *anneal* would also be performed to promote *low-resistance contacts* between the metal layer and the semiconductor.

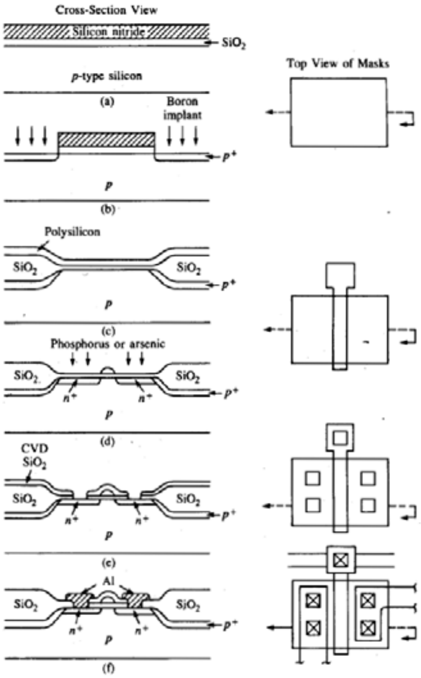
Transistor fabrication overview

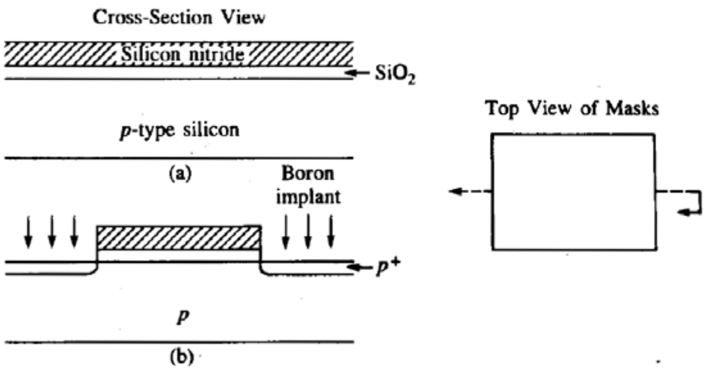
The basic structure of an n-channel metal-oxide-semiconductor (NMOS) transistor structure.

(a) The vertical cross section through the transistor.
(b) a composite top view of the masks used to fabricate the transistor in (a).



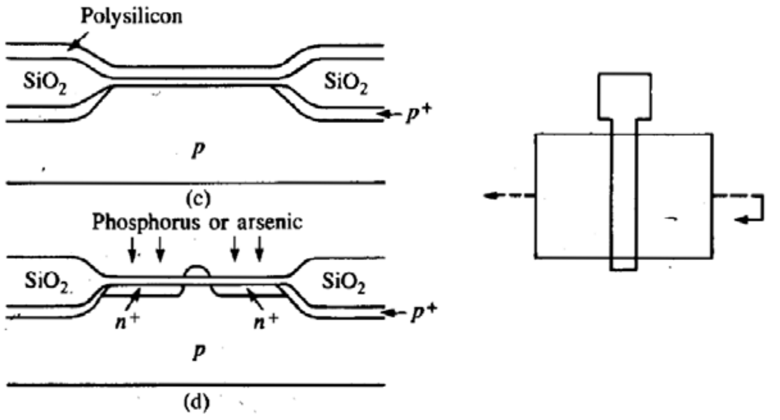
Processs sequence for a NMOS process



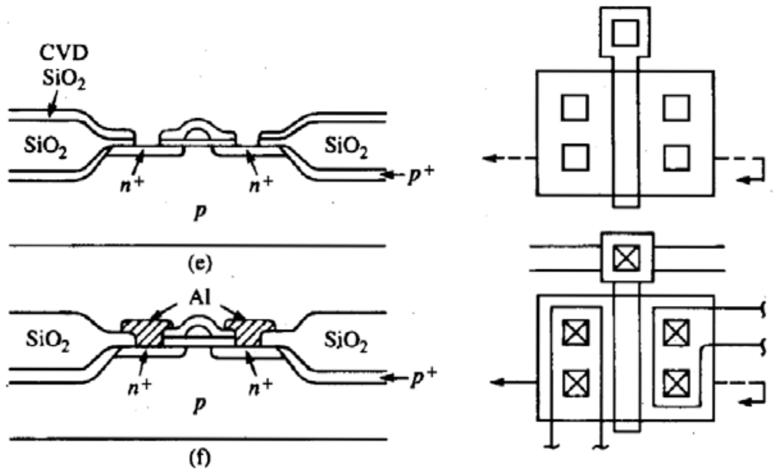


a) Silicon wafer covered with silicon nitride over a thin padding layer of silicon dioxide.

b) Etched wafer after first mask step. A boron implant is used to help control field oxide threshold.

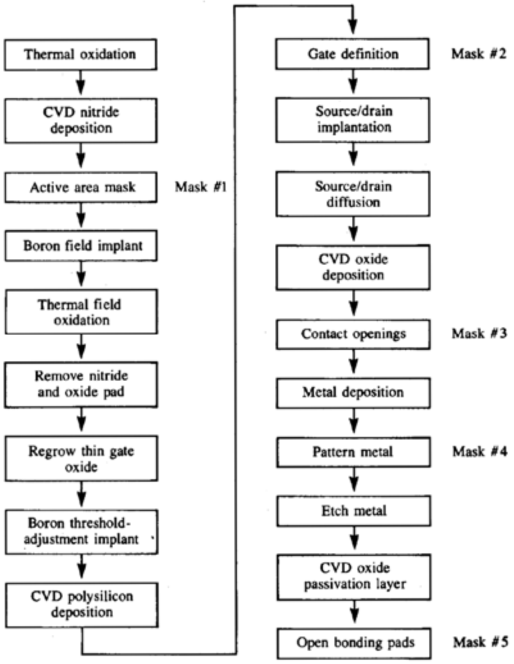


(c) Structure following nitride removal and polysilicon deposition.
(d) Wafer after second mask step and etching of polysilicon.



(e) The third mask has been used to open contact windows following silicon dioxide deposition.
(f) Final structure following metal deposition and patterning with fourth mask.

Basic NMOS process flowchart



Cross-sectional views at major steps in a basic CMOS process.

a) Following p-well diffusion.

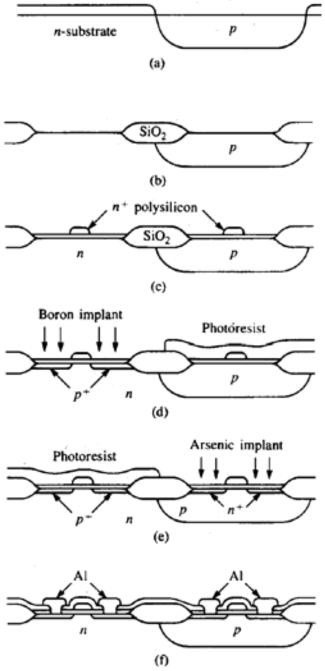
b) Following selective oxidation.

c) Following gate oxidation and polysilicon gate definition.

d) PMOS source/drain implantation;

e) NMOS source/drain implantation;

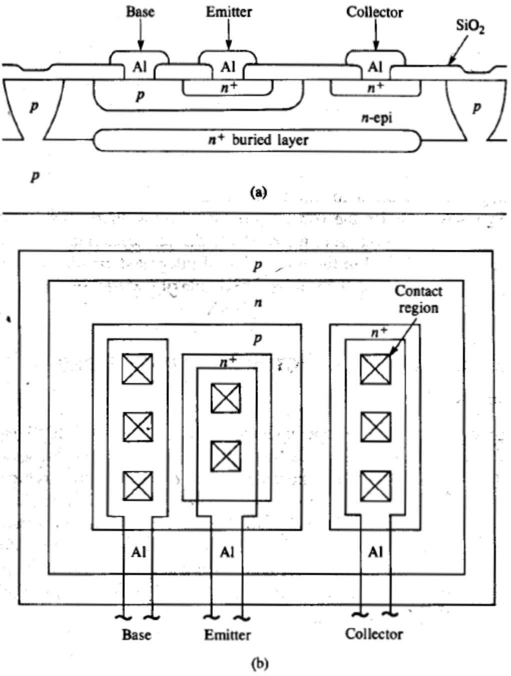
f) Structure following contact and metal mask steps.



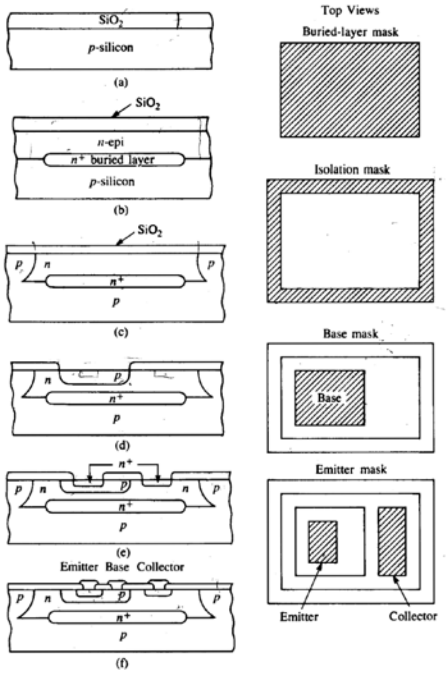
The basic structure of bipolar junction transistor (BJT)

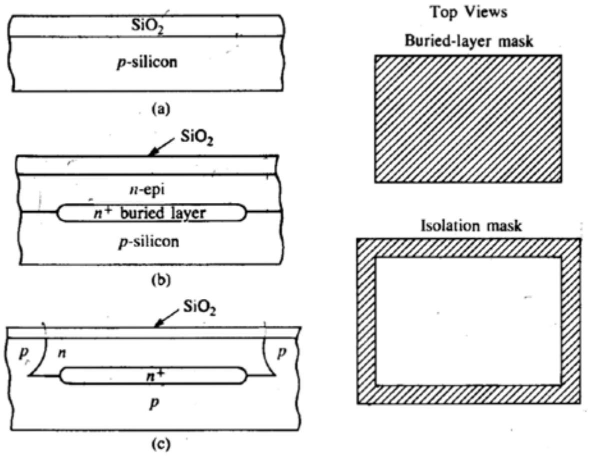
a) The vertical cross section through the transistor.

b) a composite top view of the masks used to fabricate the transistor in (a).



Cross-sectional view of the major steps in a basic bipolar process

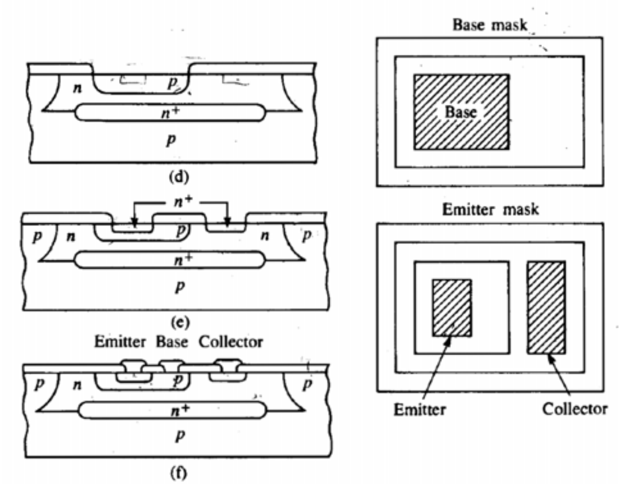




(a) Wafer with silicon dioxide layer.

(b) Following buried-layer diffusion using first mask, and subsequent epitaxial layer growth and oxidation.

(c) Following deep-isolation diffusion using second mask.

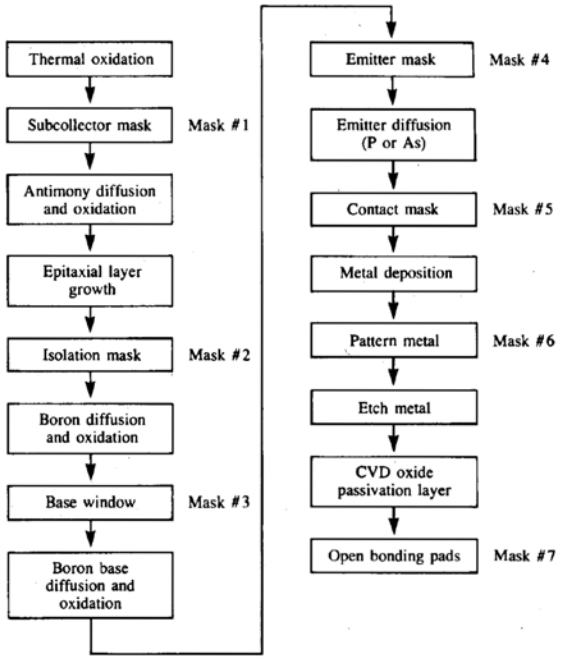


(d) Following boron-base diffusion using third mask.

(e) Fourth mask defines emitter and collector contact regions.

(f) Final structure following contact and metal mask steps.

Basic bipolar process flowchart



Introducing seminars subjects

1. CMOS technology applications
2. BiCMOS technology applications