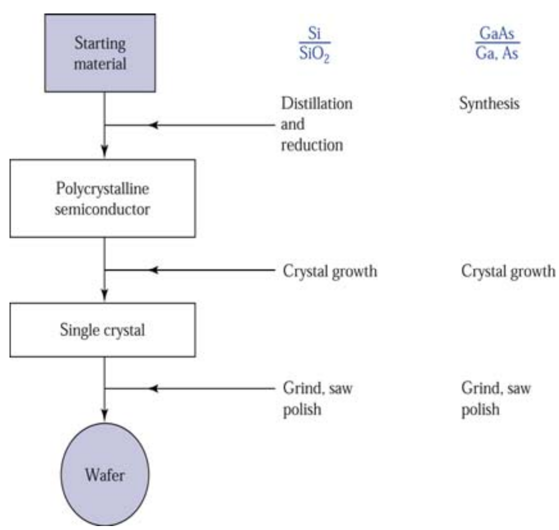
Crystal Growth

Crystal Growth

Process flow from starting material to polished wafer



Crystal Growth (Cont.)

- Forthcoming subjects:
- Basic techniques to grow silicon and GaAs single-crystal ingots
- • Wafer-shaping steps from ingots to polished wafers
- • Wafer characterization in terms of its electrical and mechanical properties

Crystal Growth (Cont.)

- The basic technique for silicon crystal growth from the melt which is material in liquid form the *Czochralski technique*.

- A *substantial percentage* (>90%) of silicon crystals for the semiconductor industry are prepared by the Czochralski technique and so is virtually all the silicon used for fabricating integrated circuits.

Starting Material

- The starting material for silicon is a relatively pure from of sand (SiO_2).
- This is placed in a furnace with various forms of carbon (coal coke and wood chips).
- Although a number of reactions take place in the furnace, the overall reaction is :

$$SiC(Solid)+SiO_2(Solid) \rightarrow Si(Solid)+SiO(Gas)+ CO(Gas)$$

Starting Material

- This process produces silicon with a purity of about 98% (Metallurgical grade Silicon(MGS)).
- Next, the silicon is treated with hydrogen chloride (HCl) at 300˚C to form trichlorosilane ($SiHCl_3$):

$$Si(Solid)+3HCl(Gas) \rightarrow SiHCl_3(gas)+H_2(Gas)$$

- Te $SiHCl_3$ is liquid in room temperature (it has a boiling point of 32˚C)
- Fractional distillation of the liquid removes the unwanted impurities.

Starting Material

- The purified $SiHCl_3$ is then used in a hydrogen reduction reaction to prepare the electronic grade silicon (EGS):

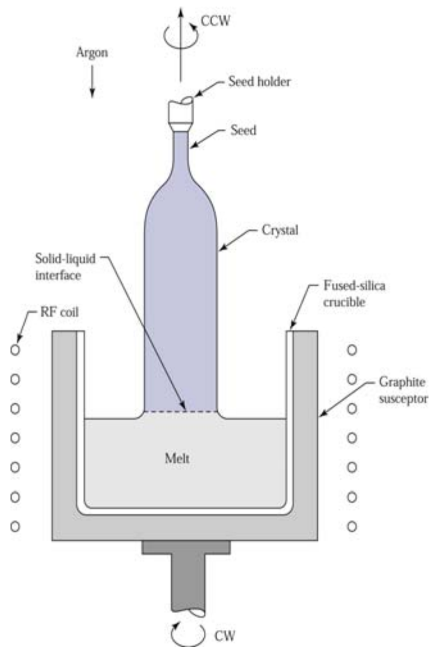
$SiHCl_3(gas) + H_2(gas) \rightarrow Si(Solid) + 3HCl(gas)$

- Pure EGS generally bas impurity concentrations in the parts-per-billion range.
- Finally polycrystalline silicon made with this technique ($3.20/kg).

The Czochralski Technique

- The Czochralski technique uses an apparatus called a *crystal puller. (fig)*
- The puller has three main components:
  a) A *furnace*, which includes a SiO_2 crucible, a graphite susceptor. a rotation mechanism a heating element and a power supply,
  b) A *crystal pulling mechanism*, which includes a seed holder and a rotation mechanism.
  c) An *ambient control*, which includes a gas source (such as argon), a flow control, and an exhaust system.

Czochralski crystal puller.
CW, clockwise;
CCW, counterclockwise.

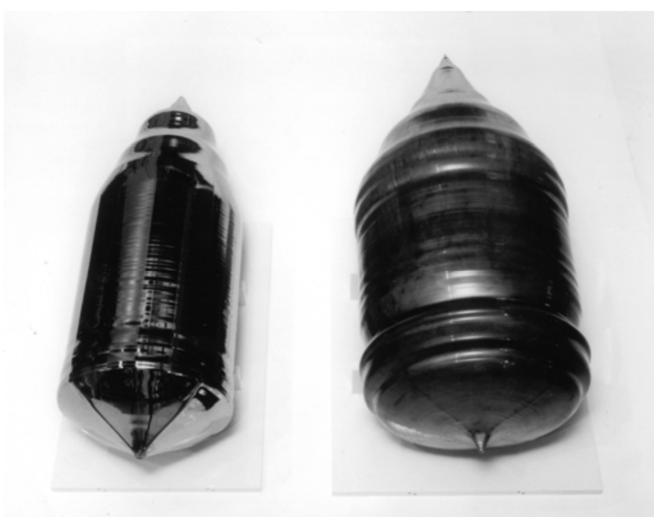


The Czochralski Technique

- The puller has an overall microprocessor-based control system to control process parameters such as temperature, crystal diameter, pull rate, and rotation speeds. as well as to permit programmed process steps. Various sensor and feedback loops allow the control system to respond automatically reducing operator intervention.
- In the crystal growing process, poly crystalline silicon (EGS) is placed in the crucible and the furnace is heated above the melting temperature of silicon. A suitably oriented seed Crystal is suspended over the crucible in a seed holder.
- The seed is inserted into the melt. Part of it melts, but tile tip of the remaining seed crystal still touches the liquid surface. It is then slowly withdrawn. Progressive freezing at the solid- liquid interface yields a large single crystal.
- A typical pull rate is a few millimeters per minute.

The Czochralski Technique

- For large-diameter silicon ingots, an external magnetic field is applied to the basic Czochralski puller. The purpose of the external magnetic field *is to control the concen*tration of defects, impurities, and oxygen.



300-mm (12 in.) and 400 mm (16 in.) Czochralski-grown silicon ingots. (Photo courtesy of Sin-Etsu Handotai Co., Tokyo.)

Distribution of Dopant

- In crystal growth, a known amount of dopant is added to the melt to obtain the desired doping concentration in the grown crystal. For silicon, boron and phosphorus are the most common dopants for *p- and n-type materials*, respectively.

- As a crystal is pulled from the melt, the doping concentration incorporated into the crystal (solid) is usually different from the doping concentration of the melt (liquid) at the interface. The ratio of these two concentrations is defined as the equilibrium *segregation coefficient*, k_o:

$$k_o = C_s / C_l$$

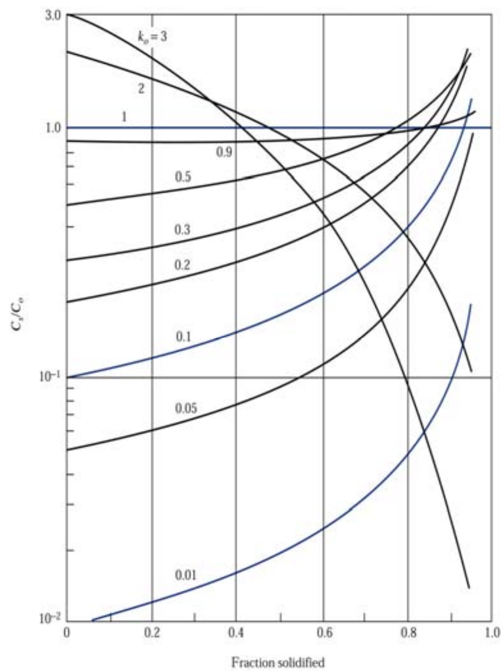
- where C_s and C_l are, respectively, the equilibrium concentrations of the dopant in the solid and liquid near the interface.

Equilibrium Segregation Coefficients for Dopants in Silicon

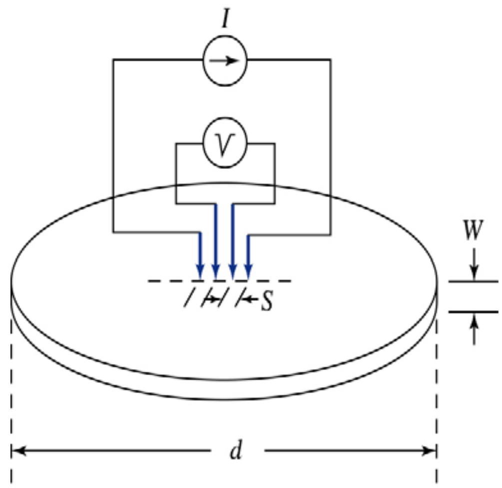
Dopant	k_0	Type	Dopant	k_0	Type
B	8×10^{-1}	p	As	3.0×10^{-1}	n
Al	2×10^{-3}	p	Sb	2.3×10^{-2}	n
Ga	8×10^{-3}	p	Te	2.0×10^{-4}	n
In	4×10^{-4}	p	Li	1.0×10^{-2}	n
O	1.25	n	Cu	4.0×10^{-4}	—[a]
C	7×10^{-2}	n	Au	2.5×10^{-5}	—[a]
P	0.35	n			

That most values are below 1 which means that during growth the dopants are *rejected in to the melt*. Consequently the melt becomes progressively enriched with the dopant as the crystal grows.

Curves for growth from the melt showing the doping concentration in a solid as a function of the fraction solidified.

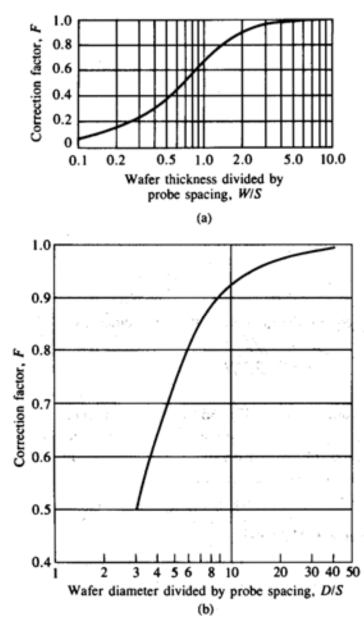


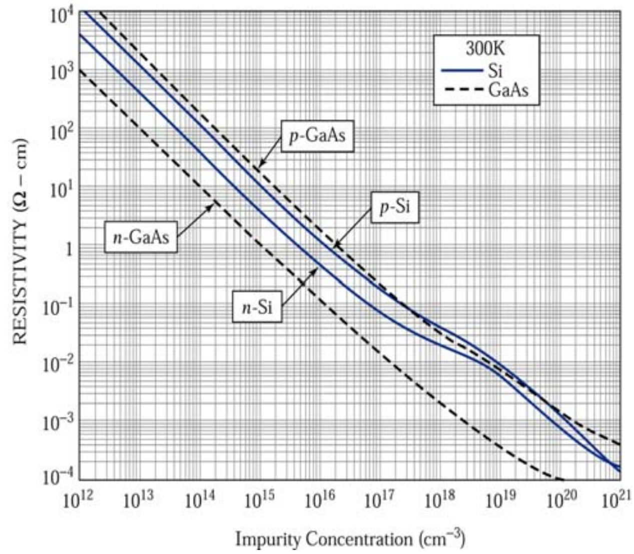
Four point probe (FPP)



Four-point probe with probe spacing used for direct measurement f bulk wafer resistivity and the sheet resistance of thin diffused layers. A known current is forced through the outer probes, and the voltage developed is measured across the inner probes.

Four-point-probe correction factors, F, used to correct for (a) wafers which are relatively thick compared to the probe spacing s and (b) wafers of finite diameter





Resistivity versus impurity concentration for Si and GaAs

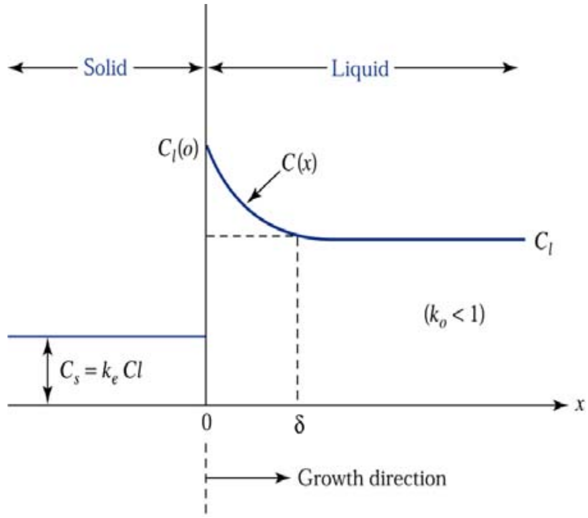
Effective Segregation Coefficient

- While the crystal is growing, dopants are constantly being rejected into the melt (for K_0<1).

- If the rejection rate is higher than the rate at which the dopant can be transported away by diffusion or stirring then a concentration gradient will develop at the interface as illustrated in Fig.

- The segregation coefficient is $k_o=C_s/C_l(0)$ we can define an effective segregation coefficient k_e *which is the ratio of* C_s *and the impurity* concentration far a-way from the interface:

$$k_e=C_s/C_l$$

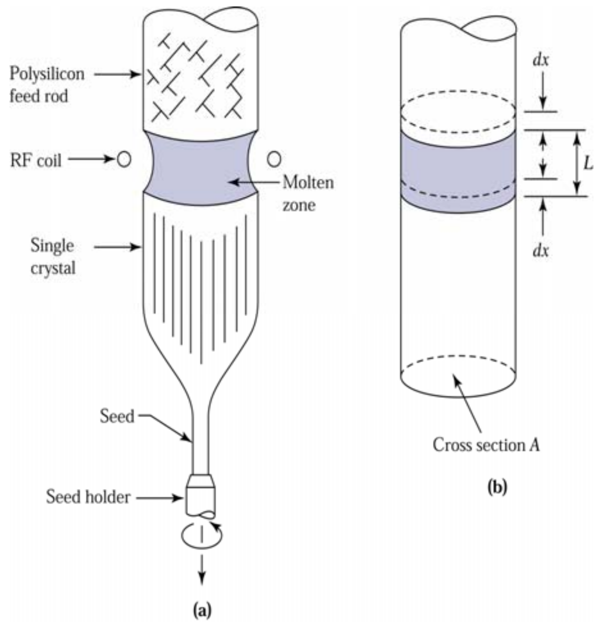


Doping distribution near the solid-melt interface

Silicon Float zone process

- Float zone process can be used to grow silicon that has *lower contamination* than that normally obtained from that Czochralski technique.
- A high purity *polycrystalline rod* with a seed crystal in the bottom is held in a vertical position and rotated (fig).
- The rod is enclosed in it quartz envelope within which an inert atmosphere (argon) is maintained. During the operation a small zone (a few centimeters in length) of the crystal is kept molten by a radio-frequency (RF) heater which is moved from the seed upward so that this floating zone transverses the length of the rod.

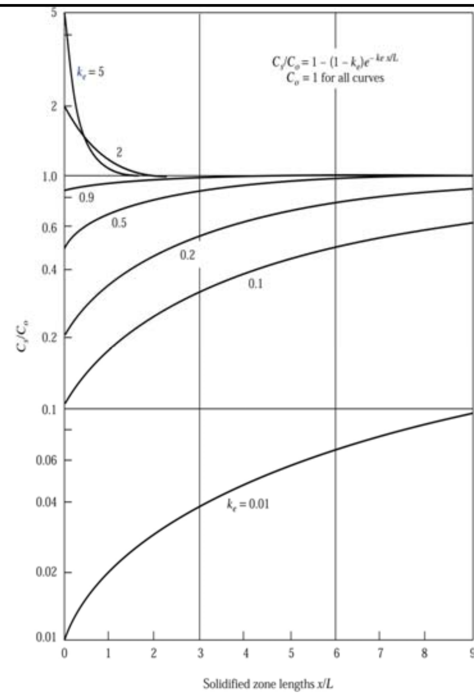
Float-zone process. (a) Schematic setup. (b) Simple model for doping evaluation.



Float zone process (Cont.)

- The molten silicon is retained by surface tension between the melting and growing solid-silicon faces. As the floating zone moves upward single crystal silicon freezes at the zone' retreating end and grows as an extension of the seed crystal.
- Materials with higher resistivity can be obtained from the zone. process than from the Czochralski process because the former can be used to purify the crystal more easily.
- Furthermore, since no crucible is used in the float-zone process, there is no contamination from the crucible (as with Czochralski growth). At the present time, Float-zone crystals are used mainly for high power high voltage devices. where high-resistivity materials are required.

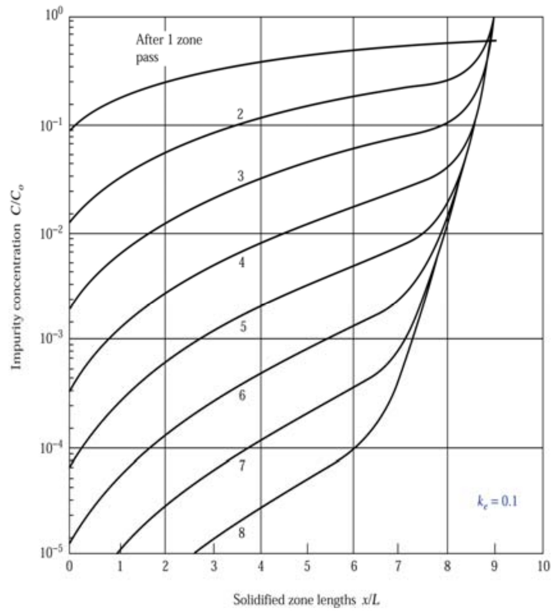
Curves for the float-zone process showing doping concentration in the solid as a function of solidified zone lengths.[4]

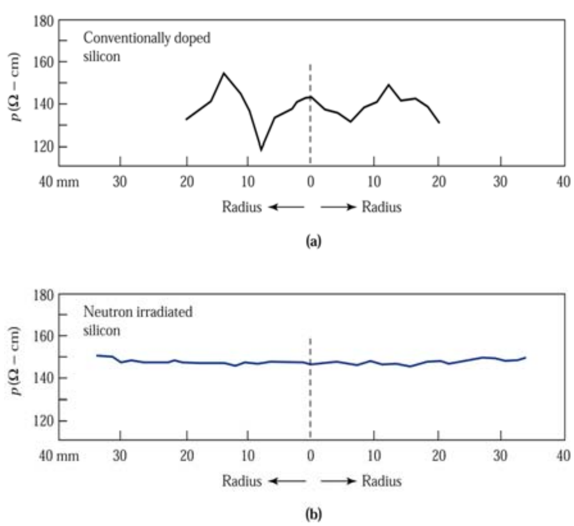


Float zone process (Cont.)

- These two crystal growth techniques can also be used to *remove impurities*.
- A single pass in the float-zone process does not produce as much purification as a single Czochralski growth. But by *repeating the float zone process* more purify silicon can be achieved.

Relative impurity concentration versus zone length for a number of passes. *L* denotes the zone length.

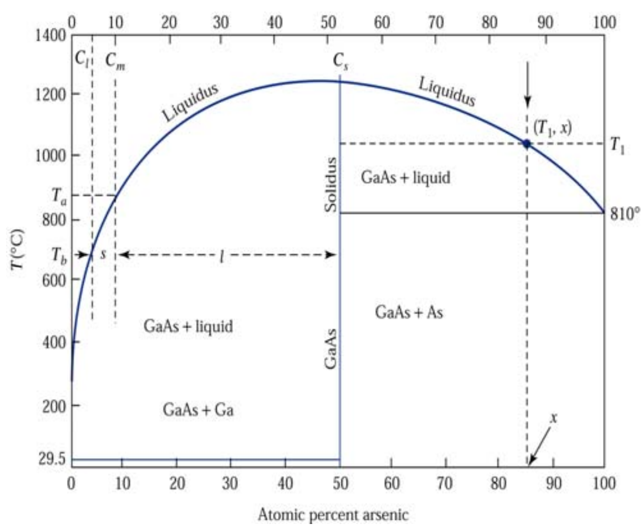




(*a*) Typical lateral resistivity distribution in a conventionally doped silicon.
(*b*) Silicon doped by neutron irradiation.

GaAs CRYSTAL GROWTH TECHNIQUES

- Starting Materials
  - The starting materials for the synthesis of *polycrystalline gallium arsenide* are the elemental chemical pure gallium and arsenic. Because gallium arsenide is a *combination of two materials*, its behavior is different from that of a single material such as silicon.
  - The behavior of a combination com be described by a *phase diagram*.
  - A phase diagram shows the relationship between the two components, gallium and arsenic as a function of *temperature*.

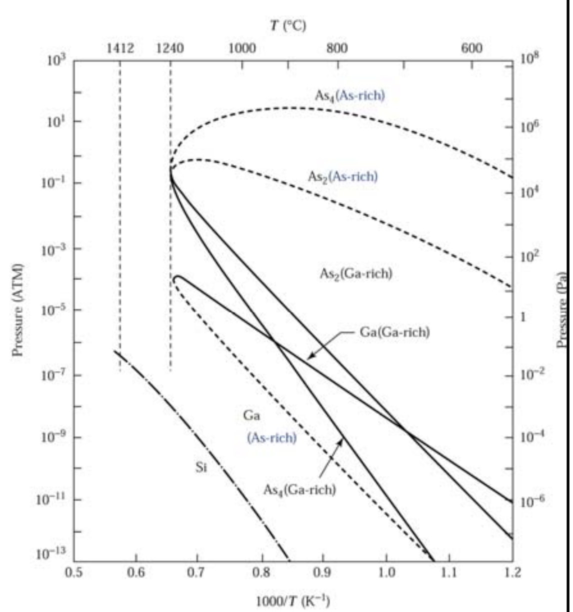


Phase diagram for the gallium-arsenic system.

Starting material (cont.)

- Consider a melt that is initial , of composition *x (e.g 85 atomic percent arsenic. as shown in Fig. 2.10). then the temperature is lowered,* its composition will remain fixed until liquidus line is reached. At the point *(T_1, x),* material of 50 atomic percent arsenic (i.e . gallium arsenide) will begin to solidify.

Partial pressure of gallium and arsenic over gallium arsenide as a function of temperature. Also shown is the partial pressure of silicon



GaAs Polycrystall

- To synthesize gallium arsenide an **evacuated sealed quartz tube system** with a two temperature furnace is commonly used. The high-purity arsenic is placed in graphite boat and heated to 610°C to 620°C, whereas the high-purity gallium is placed in another graphite boat and heated to slightly above the gallium arsenide melting temperature (1240~1 260°C).

- Under these conditions an overpressure of arsenic is established :
  - to cause the **transport of arsenic vapor to the gallium melt** converting into *gallium arsenide*.
  - to prevent **decomposition of the gallium arsenide** while it is being formed in the furnace.

- When the melt ***cools*** high-purity polycrystalline gallium arsenide results. This serves as the raw material to grow single-crystal gallium arsenide

Crystal Growth techniques

- There are two techniques for GaAs growth technique:
  - **Czochralski**→ more popular for large diameter ingot.
  - **Bridgeman**→ Most GaAs is grown by this technique.

- For **Czochralski** growth of gallium arsenide, the basic puller is identical to that for silicon. However to prevent decomposition of the melt during crystal growth, a liquid encapsulation is employed.

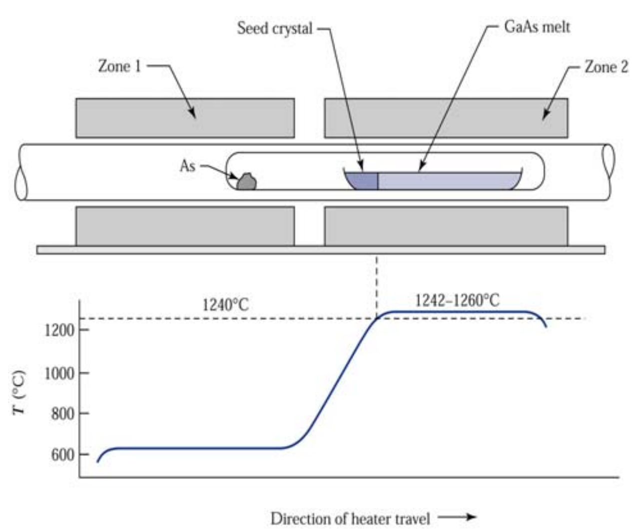
- The liquid encapsulant is a **molten boron trioxide (B2O3)** layer about **1 cm** thick. Molten boron trioxide is inert to the gallium arsenide surface and serves as a cap to cover the melt. This cap prevents decomposition or the gallium arsenide as long as the pressure on its surface is higher than 1 atm (760 Torr). Because boron trioxide can dissolve silicon dioxide the silica crucible is replaced with a graphite crucible.

Crystal Growth techniques

- GaAs doping
  - Cadmium and Zinc → p type
  - Selenium, Silicon and Tellurium → n type

- The expressions derived previously for Si are equally applicable to GaAs.

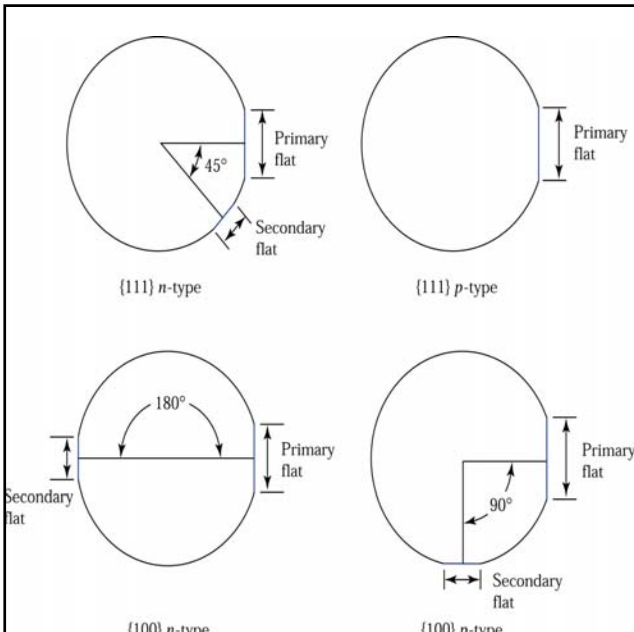
- In Bridgeman technique the impurity distribution can be described as before and the growth rate is given by the traversing speed or the furnace.



Bridgeman technique for growing single-crystal gallium arsenide and a temperature profile of the furnace.

MATERIAL CHARACTERIZATION

- **Wafer Shaping:**
  1. Removing the seed and the other end of the ingot, which is last to solidify.
  2. Grinding the surface so that the diameter of the material is defined.
  3. One or more **flat regions** are ground along the length of the ingot. These regions, or flats, marks the specific **crystal orientation** or the ingot and the **conductivity type** or the material.
     - After that The largest flat, the primary flat allows a mechanical locator in automatic processing equipment to position the wafer and to orient die devices related to the crystal.
     - Other smaller flats, called secondary flats, are ground to identify the orientation and conductivity type of the crystal, as shown in Figure.



Identifying flats on a semiconductor wafer.

Wafer shaping (Cont.)

- The ingot is then ready to be sliced by diamond saw into wafers. Slicing determines four wafer parameters:
  1. *Surface orientation (e.g. < 111 > or <100>);*
  2. *Thickness (e.g. 0.5-0.7 mm) , depending on wafer diameter);*
  3. *Taper, which is the wafer thickness variations from one end to another;*
  4. *Bow, which is the surface curvature of the wafer, measured from the center of the wafer to its edge.*

Wafer shaping

- After slicing both sides of the wafer are lapped using a mixture of $Al_2 0_3$ and glycerin to produce a typical flatness uniformity.
- The final step of wafer shaping is polishing. Its purpose is to provide a smooth surface where device features can be defined by photolithographic processes.
- For large crystals (>200 mm diameter), no flats are ground instead; a groove is made on the edge of the wafer for positioning and orientation purposes.


200-mm (8 in.) and 400-mm (16 in.) polished silicon wafers in cassettes. (Photo courtesy of Sin-Etsu Handotai Co., Tokyo.)

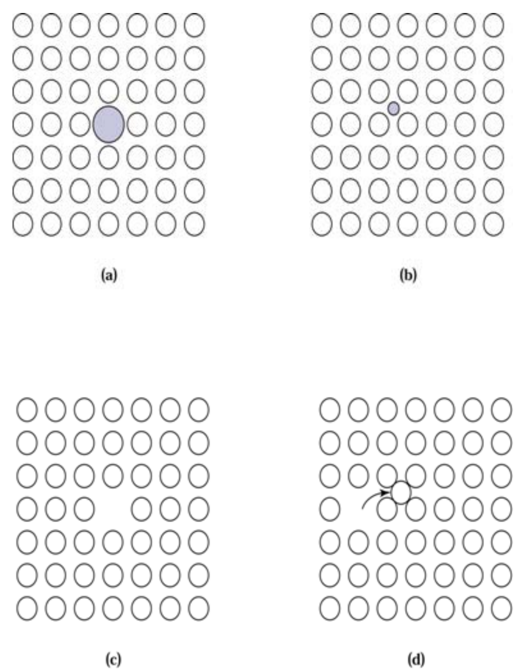
TABLE 2.3 Specifications for Polished Monocrystalline Silicon Wafers

Parameter	125 mm	150 mm	200 mm	300 mm
Diameter (mm)	125 ± 1	150 ± 1	200 ± 1	300 ± 1
Thickness (mm)	0.6–0.65	0.65–0.7	0.715–0.735	0.755–0.775
Primary flat length (mm)	40–45	55–60	NA	NA
Secondary flat length (mm)	25–30	35–40	NA	NA
Bow (μm)	70	60	30	< 30
Total thickness variation (μm)	65	50	10	< 10
Surface orientation	(100) ± 1°	Same	Same	Same
	(111) ± 1°	Same	Same	Same

NA, not available.

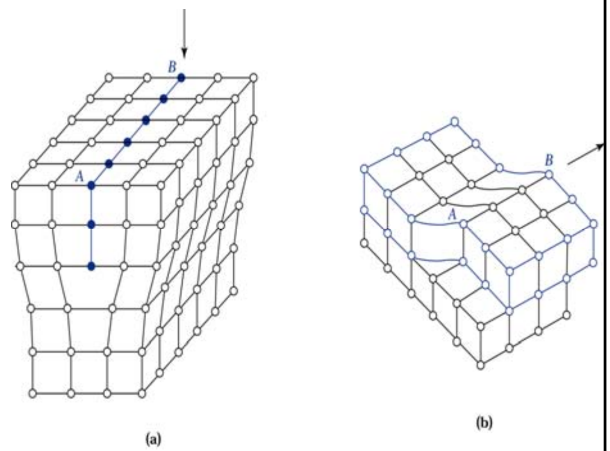
Crystal Characterization

- **Crystal Defects:**
- A real crystal (such as a silicon wafer) differs from the ideal crystal in important ways.
  - It is **finite**; thus, surface atoms are incompletely bonded.
  - It has **defects**, which strongly influence the electrical, mechanical, and optical properties of the semiconductor.
- Categories of defects:
  - *point* defects, *line* defects, *area* defects and *volume* defects.

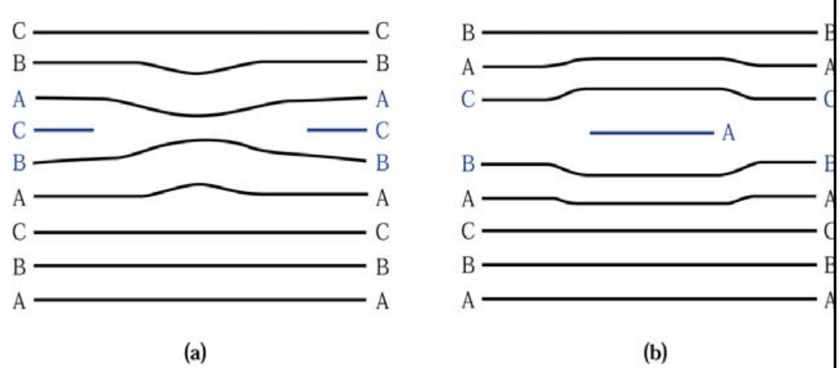


Point defects.
(a) Substitutional impurity.
(b) Interstitial impurity.
(c) Lattice vacancy.
(d) Frenkel-type defect.

Point defects are particularly important subjects in the kinetics of oxidation and diffusion processes.



Line defects
(*a*) Edge dislocation formation in cubic crystals.
(*b*) screw dislocation formation in cubic crystals.
They act as precipitation sites for metallic impurities. which may degrade device performance.



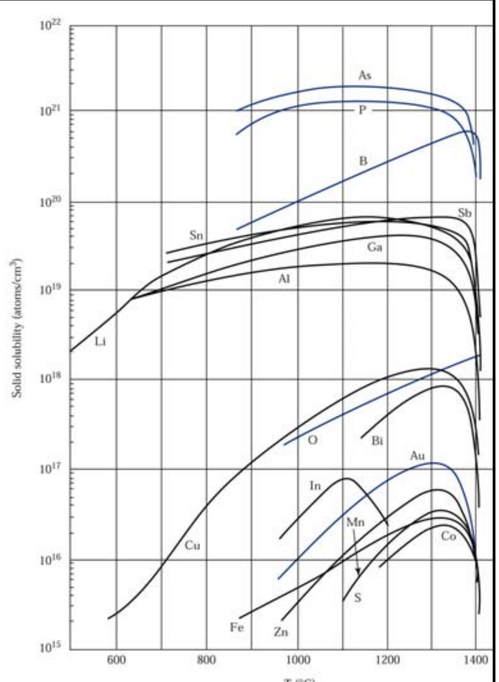
Area defects (Stacking fault in semiconductor)
(*a*) Intrinsic stacking fault.
(*b*) Extrinsic stacking fault.

In this defect, the stacking sequence of an atomic layer is interrupted. Such defects may appear during crystal growth. Crystals having these area defects are **not** usable for integrated circuit manufacture and are discarded.

Volume defect

- impurities or dopants atoms make up the fourth class of defects.
- These defects arise because of the inherent solubility of tile impurity in the host lattice.

Solid solubilities of impurity elements in silicon.



Material Properties

TABLE 2.4 Comparison of Silicon Material Characteristics and Requirements for ULSI

Property	Characteristics		Requirements for ULSI
	Czochralski	Float Zone	
Resistivity (phosphorus) *n*-type (ohm-cm)	1–50	1–300 and up	5–50 and up
Resistivity (antimony) *n*-type (ohm-cm)	0.005–10	—	0.001–0.02
Resistivity (boron) *p*-type (ohm-cm)	0.005–50	1–300	5–50 and up
Resistivity gradient (four-point probe) (%)	5–10	20	< 1
Minority carrier lifetime (μs)	30–300	50–500	300–1000
Oxygen (ppma)	5–25	Not detected	Uniform and controlled
Carbon (ppma)	1–5	0.1–1	< 0.1
Dislocation (before processing) (per cm^2)	≤ 500	≤ 500	≤ 1
Diameter (mm)	Up to 200	Up to 100	Up to 300
Slice bow (μm)	≤ 25	≤ 25	< 5
Slice taper (μm)	≤ 15	≤ 15	< 5
Surface flatness (μm)	≤ 5	≤ 5	< 1
Heavy-metal impurities (ppba)	≤ 1	≤ 0.01	< 0.001

ppma, parts per million atoms; ppba, parts per billion atoms.

Introducing course project

- Molecular Beam Epitaxy (MBE)
- Metalorganic Chemical Vapor Epitaxy (MOCVD)

Material Properties (Cont.)

- The resistivity is measured by the four-point probe method.
- Minority carrier life time measured by photoconductivity method.
- trace impurities such as oxygen and carbon in silicon can be analyzed by the secondary ion mass spectroscopic (SIMS) technique.
- The oxygen and carbon concentrations are substantially higher in Czochralski method than in float-zone crystals because of the dissolution of oxygen from the silica crucible and transport of carbon to the melt from the graphite susceptor during crystal growth.

Material Properties (Cont.)

- The presence of carbon is undesirable because it aids the formation of *defects*.
- Oxygen, however, has both deleterious and beneficial effects.
  - It can act as a donor. distorting the resistivity of the crystal caused by intentional doping.
  - On the other hand, oxygen in an interstitial lattice site can increase the yield strength of silicon.